

Attorney's Docket No.: 14580-031001

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

This application has been amended to place it in a full condition for allowance. The description has been amended to reflect the newly amended Claim 1. In addition, Claims 1, 4 and 5 have been amended. No new matter is added. Claims 1 and 3-10 remain pending and are patentable, at a minimum, for the reasons stated below.

1. Claim Objections

All objections to claims have been obviated by the above amendments.

2. Claim Rejections under 35 USC 112, Second Paragraph

Claim 1 has been amended to recite "etching the ferroelectric layer and the layer of the second electrically insulating material to form isolated ferroelectric elements which have exposed side surfaces." The underlined portion that has now been added to Claim 1 fully addresses the rejection raised in the Final Office Action. Hence, Claims 1, 6, 9 and 10 are patentable under 35 USC 112, second paragraph.

3. Claim Rejections under 35 USC 102(e) over Kanaya

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Claims 1-6, 8 and 10 stand rejected under 35 USC 102(e) as being anticipated by Kanaya. This contention, however, is respectfully traversed because Kanaya fails to teach each feature in these claims.

In Kanaya, the method steps for forming a ferroelectric capacitor are described to be as follows:

1. an insulating layer of silicon dioxide is applied to a substrate;
2. a layer of aluminum oxide is applied to the layer of silicon dioxide as a hydrogen barrier;
3. a layer of platinum is applied to the layer of aluminum oxide to act as a first electrode;
4. a layer of PZT is applied to the layer of platinum;
5. an annealing step is then performed to crystallize the ferroelectric material;
6. a second layer of platinum is applied to the crystallized layer of PZT which acts as a second electrode;
7. a layer of aluminum oxide is applied to the second layer of platinum to act as a hydrogen barrier;
8. a layer of silicon dioxide is applied to the layer of aluminum oxide to act as a mask;
9. a resist pattern is applied;

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10. an etching process is performed such that the layers down to but not including the layer of ferroelectric material (PZT) are etched;

11. a layer of silicon dioxide is removed and a layer of aluminum oxide is applied, and

12. a second etching process is performed for etching the PZT layers and the substrate to form the capacitor.

The above process in Kanaya places the PZT layer 4 in direct contact and between two electrically conductive Pt layers 3 and 5 as illustrated in the cited FIG. 18 and other figures in Kanaya.

Kanaya's process and the resultant structure by the process, however, are very different from the process and the associated structures in Claims 1-6, 8 and 10 of this application.

First, Claims 1-6, 8 and 10 recite, among other features, the following depositing steps:

*depositing a ferroelectric layer of amorphous ferroelectric material directly on a layer of a first electrically insulating material;*

*depositing a layer of a second electrically insulating material to cover the ferroelectric layer;*

Hence, the methods in Claims 1-6, 8 and 10 deposit the ferroelectric layer between layer of the first electrically

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insulating material and the layer of the second electrically insulating material.

In stark contrast, Kanaya's process deposit the PZT layer 4 in direct contact and between two electrically conductive Pt layers 3 and 5 (FIG. 18). For this reason alone, the portion in Kanaya as cited by the Final Office Action fails to anticipate Claims 1-6, 8 and 10 and the rejections under 35 USC 102(e) must be withdrawn. Therefore, Claims 1-6, 8 and 10 are patentable over Kanaya.

Second, Claims 1-6, 8 and 10 recites "providing a layer of a conductive material in contact with each of the side surfaces." See, Figure 1 of this application where the layer 9 is an example of the recited conductive layer and the layers 5 and 7 are examples of the recited layers of the first and second electrically insulating materials, respectively.

Kanaya, however, teaches depositing an interlayer insulating film 6a that is in contact with each side surface of the PZT layer 4 in FIG. 18. Therefore, the cited portion in Kanaya in the Final Office Action fails to teach, once again, each feature in Claims 1-6, 8 and 10.

In this regard, Claim 1 is further amended to recite that the exposed side surfaces of isolated ferroelectric elements are substantially perpendicular to the ferroelectric layer. As an example, Figure 1 of this application shows the conductive layer

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9 on the side surface of the PZT element 5 is perpendicular to the original PZT layer prior to formation of the isolated PZT elements 5. In Kanaya, the twoelectrically conductive Pt layers 3 and 5 are parallel to, rather than perpendicular to, the PZT layer 5.

Therefore, this difference provides another ground why Claims 1-6, 8 and 10 are distinctly different from Kanaya and thus are patentable over Kanaya.

In fact, Claims 1-6, 8 and 10 recite methods that form a vertical ferroelectric capacitor where the vertical direction is the direction perpendicular to the PZT layer. By contrast, in Kanaya the capacitor formed is a horizontal capacitor that is completely different from the vertical capacitor. The undersigned asks the Examiner to compare Figure 1 of this application and the cited FIG. 18 in Kanaya to see the two very different capacitor structures produced by the very different methods.

Claims 1-6, 8 and 10 also differ from Kanaya in other aspects. For example, Claims 1-6, 8 and 10 recite etching the ferroelectric layer and the second electrically insulating material to form isolated ferroelectric elements which have exposed side surfaces. By contrast, the etching in Kanaya is not to form isolated ferroelectric elements but instead is to form the whole capacitor.

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For another example, Claims 1-6, 8 and 10 recite performing an annealing step to crystallize the ferroelectric material, the conductive material promoting crystallization of the ferroelectric material to a higher degree than the first and second electrically insulating materials, whereby the crystallization proceeds substantially horizontally through each of the ferroelectric elements. Kanaya, in contrast, fails to provide disclosure or teaching of the conductive material (which in Kanaya is not in any event in contact with the side surfaces) promoting crystallization of the ferroelectric material to a higher degree than the first and second electrically insulating materials.

For at least the above reasons, Claims 1-6, 8 and 10 are patentable under 35 USC 102(e) over Kanaya.

In addition, claim rejections under 35 USC 103(a) over Kanaya must also be withdrawn for the above absence of teaching of various features in the present claims.

In addition, the present claims are patentable over Kanaya for other reasons. As an example, Kanaya is not concerned with crystallization of the ferroelectric layer. The present claims, in contrast, recite crystallization of the ferroelectric layer. In this regard, Kanaya is directed to solving problems caused by the effects of hydrogen diffusion and the solution taught is the provision of a hydrogen barrier layer to inhibit such diffusion.

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There is no disclosure or teaching in Kanaya of providing a material at the sides of the ferroelectric layer to promote crystallization more than the material above and below the ferroelectric layer so that crystallization proceeds horizontally, a feature of the present invention defined by claim 1. Furthermore, there is no disclosure or suggestion in Kanaya of the advantages of such features which have been appreciated by the present applicant.

For at least the reasons stated above, it is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

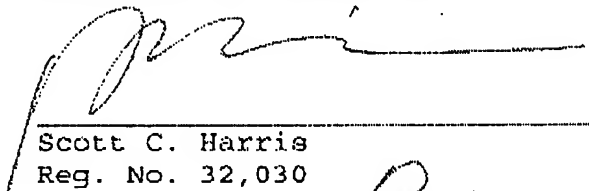
Applicants ask that all claims be allowed. Please apply the RCE fee in the amount of \$790, the one month extension of

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time fee in the amount of \$120, and any other applicable charges  
or credits, to Deposit Account No. 06-1050.

Respectfully submitted,

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